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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/074,816	02/13/2002	Neil Clair Berglund	ROC920010293US1	7132

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EXAMINER	
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ART UNIT	PAPER NUMBER
2154	

DATE MAILED: 04/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/074,816	BERGLUND ET AL.	
	Examiner	Art Unit	
	Ashok B. Patel	2154	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/13/2002*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Application Number 10/074, 816 was filed on 02/13/2002. Claims 1-29 are subject to examination.

Claim Objections

2. Claim 22 is objected to because of the following informalities: Line 3 of this claim contains the word "bus" which seems to be required to be "busy". Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless-

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-7, 10-21, and 24-29 are rejected under 35 U.S.C. 102(e) as being anticipated by Ip (US 2003/0046339 A1).

Referring to claim 1,

The reference teaches an apparatus for holding one or more devices (Fig. 1, element 10a), comprising:

a rack (Fig. 1, element 10a) comprising:

one or more device, at least one device having a microcontroller (page 2, para. [0024], "A data collection unit 30 is preferably associated with each rack 10 or

is otherwise associated with a group of servers 15.");

a device memory associated with the at least one device, the device memory containing a unique identifier (page 2, para. [0024]); and

a bus connecting the microcontroller and the device memory, the microcontroller being configured to retrieve the unique identifier (page 2, para. [0024], "A data collection unit 30 is preferably associated with each rack 10 or is otherwise associated with a group of servers 15.", page 3, para. [0030]," Communication circuit 50 is preferably a web server circuit. A web server circuit is essentially a web server that is implemented as a single microcontroller or programmable interrupt controller (PIC).").

Referring to claim 2,

The reference teaches the apparatus of claim 1, wherein the device memory comprises information about the device. (page 2, para. [0024]);

Referring to claim 3,

The reference teaches the apparatus of claim 1, wherein the rack further comprising a rack memory connected to the microcontroller through the bus (Fig. 1, element 30a), the rack memory containing information about the rack (page 2, para. [0024]); and the microcontroller being configured to retrieve the information from the rack memory (page 3, para. [0030]).

Referring to claim 4,

The reference teaches the apparatus of claim 1, wherein information about the rack comprises a unique identifier associated with the rack. (page 2, para. [0024])

Referring to claim 5,

The reference teaches the apparatus of claim 1, wherein the device further comprises a user interface communicably linked to the microcontroller. (Fig.1, element 60 and 65)

Referring to claim 6,

The reference teaches the apparatus of claim 1, wherein the microcontroller is communicably linked to a user interface. (Fig.1, element 60 and 65).

Referring to claim 7,

The reference teaches the apparatus of claim 6, wherein the user interface is remote from the rack. (Fig.1, element 60 and 65, page 4, para. [0032]).

Referring to claim 10,

The reference teaches the apparatus of claim 6, wherein the microcontroller contains a device-inventory program; and a processor which, when executing the device-inventory program, performs an operation comprising:

receiving a request command from the user interface;

issuing a retrieve command to the device memory in response to receiving the request command, the retrieve command being configured to retrieve information about the device;

receiving the information about the device; and sending the information about the device to the user interface. (page 3, para.[0029],[0030], page 4, para.[0031],[0032])

Referring to claim 11,

The reference teaches an apparatus for holding one or more devices (Fig.1, element 10a), comprising:

a rack (Fig.1, element 10a) comprising:

one or more device, at least one device having a microcontroller (page 2, para. [0024]," "A data collection unit 30 is preferably associated with each rack 10 or is otherwise associated with a group of servers 15.");

a rack memory associated with the at least one device, the rack memory containing information about the rack (Fig.1, element 30a); and

a bus connecting the microcontroller and the rack memory, the microcontroller being configured to retrieve the unique identifier. (page 2, para. [0024], "A data collection unit 30 is preferably associated with each rack 10 or is otherwise associated with a group of servers 15.", page 3, para. [0030]," Communication circuit 50 is preferably a web server circuit. A web server circuit is essentially a web server that is implemented as a single microcontroller or programmable interrupt controller (PIC)." page 3, para. [0029], page 4, para. [0031], [0032]).

Referring to claim 12,

The reference teaches the apparatus of claim 11, wherein the information about the rack comprises a unique identifier associated with the rack. (page 2, para. [0024])

Referring to claim 13,

The reference teaches a microcontroller (Fig.1, element 30a), comprising:

a memory containing a device-inventory program; and

a processor which, when executing the device-inventory program, performs an operation comprising:

receiving a request command (page 3, para. [0025])

issuing a retrieve command to one or more memories connected to the microcontroller in response to receiving the request command, the retrieve command being configured to retrieve inventory information from the one or more memories; receiving the inventory information from the one or more memories, the inventory information containing one of information about a device and information about a rack; and sending the inventory information to the user interface. (Fig. 1, element 60 and 65, page 3, para.[0025],[0029],[0030],, page 4, para.[0031],[0032]).

Referring to claim 14,

The reference teaches a method of programmatically taking an inventory of one or more devices, each device being mounted on a rack (Fig. 1), comprising:

receiving a request command from a user interface (Fig. 1, element 60 and 65) communicably linked to a microcontroller (Fig. 1, element 30a);

issuing a retrieve command to one or more memories connected to the microcontroller in response to receiving the request command, the retrieve command being configured to retrieve inventory information from the one or more memories; receiving the inventory information from the one or more memories; and sending the inventory information to the user interface. (page 3, para.[0025],[0029],[0030],, page 4, para.[0031],[0032]).

Referring to claim 15,

The reference teaches the method of claim 14, wherein the request command is configured to request the microcontroller to issue the retrieve command to the one or more memories. (page 2, para.[0027]).

Referring to claim 16,

The reference teaches the method of claim 14, wherein the one or more memories comprise one or more device memories, each device memory being coupled to one of the rack and a device. (Fig. 1, elements 15a, 30a, 10a).

Referring to claim 17,

The reference teaches the method of claim 16, wherein each device memory comprises the inventory information containing one of a unique identifier associated with the device and information about the device. (Page 2, para. [0024])

Referring to claim 18,

The reference teaches the method of claim 14, wherein the one or more memories comprise a rack memory coupled to the rack. (Fig. 1, elements 15a, 30a)

Referring to claim 19,

The reference teaches the method of claim 18, wherein the rack memory comprises the inventory information containing one of a unique identifier associated with the rack and information about the rack. (Page 2, para. [0024])

Referring to claim 20,

The reference teaches the method of claim 14, wherein the microcontroller is connected to one of the rack and at least one of the one or more devices. (Fig. 1, elements 15a, 30a)

Referring to claim 21,

The reference teaches the method of claim 14, wherein the retrieve command is issued

by the microcontroller to the one or more memories through a bus. (Page 2, para. [0024]," A data collection unit 30 is preferably associated with each rack 10 or is otherwise associated with a group of servers 15. The data collection unit 30 may be mounted on rack 10.")

Referring to claim 24,

Claim 24 is a claim to a computer-readable medium containing a program which, when executed by a processor, performs the method of claim 14. Therefore claim 24 is rejected for the reasons set forth for claim 14.

Referring to claim 25,

Claim 25 is a claim to the computer-readable medium containing a program which, when executed by a processor, performs the method of claim 15. Therefore claim 25 is rejected for the reasons set forth for claim 15.

Referring to claim 26,

Claim 26 is a claim to the computer-readable medium containing a program which, when executed by a processor, performs the method of claim 16. Therefore claim 26 is rejected for the reasons set forth for claim 16.

Referring to claim 27,

Claim 27 is a claim to the computer-readable medium containing a program which, when executed by a processor, performs the method of claim 17. Therefore claim 27 is rejected for the reasons set forth for claim 17.

Referring to claim 28,

Claim 28 is a claim to a computer-readable medium containing a program which, when executed by a processor, performs the method of claim 18. Therefore claim 28 is rejected for the reasons set forth for claim 18.

Referring to claim 29,

Claim 29 is a claim to a computer-readable medium containing a program which, when executed by a processor, performs the method of claim 19. Therefore claim 29 is rejected for the reasons set forth for claim 19.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 8, 9, 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. Ip (hereinafter Ip) (US 2003/0046339 A1) in view of Little et al. (herein after Little) (pub. No. US 2001/0011353 A1)

Referring to claims 8 and 9,

Keeping in mind the teachings of the reference Ip as stated above, the reference Ip fails to explicitly teach the apparatus of claim 1, wherein the bus is a one-wire bus, and the apparatus of claim 1, wherein the bus comprises a wire configured to indicate to the microcontroller that the bus is busy.

The reference Little teaches at page 4, para. [0049], "It is understood that the present invention is not limited to a single wire connection between a master/host and the electronic module. Furthermore, the present invention is not limited to the one wire protocol for communication over a single wire. The present invention could use more than one wire to communicate between the electronic module and the master. You could use two, three, five or more wires to communicate. It is preferred that a single wire or connection is used because a single wire connection is less expensive to manufacture and can be made much more durable than a multiple wire connection."

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to employ a single wire bus for communication between the data collector and the servers in the rack of Ip such that a master/host communication is established between them and also a second wire be installed to communicate other status such as the "bus is busy." It would have been obvious because lesser number of connections are not only less expensive to manufacture but also much more durable than a multiple wire connection as taught by Little.

Referring to claims 22 and 23,

Keeping in mind the teachings of the reference Ip as stated above, although the reference teaches the method of claim 22, wherein the another retrieve command is issued after a random period of time. (page 6, para. [0044]), the reference fails to explicitly teach method of claim 14, wherein issuing the retrieve command comprises: determining whether a busy message exists; and if the busy message exists, then issuing another retrieve command to the one or more memories.

The reference Little teaches at page 4, para. [0049], "It is understood that the present invention is not limited to a single wire connection between a master/host and the electronic module. Furthermore, the present invention is not limited to the one wire protocol for communication over a single wire. The present invention could use more than one wire to communicate between the electronic module and the master. You could use two, three, five or more wires to communicate. It is preferred that a single wire or connection is used because a single wire connection is less expensive to manufacture and can be made much more durable than a multiple wire connection."

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to employ a single wire bus for communication between the data collector and the servers in the rack of Ip such that a master/host communication is established between them and also a second wire be installed to communicate other status such as the "bus is busy."

It would have been obvious because lesser number of connections are not only less expensive to manufacture but also much more durable than a multiple wire connection as taught by Little.

Conclusion

Examiner's note: Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses,

to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ashok B. Patel whose telephone number is (571) 272-3972. The examiner can normally be reached on 8:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John A Follansbee can be reached on (571) 272-3964. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Abp
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